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UNITED STATES PATENT APPLICATION

FOR

TECHNIQUES TO PROVIDE INCREASED VOLTAGE SWINGS IN OSCILLATORS

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TECHNIQUES TO PROVIDE INCREASED VOLTAGE SWINGS IN OSCILLATORS

Field

[0001] The subject matter disclosed herein generally relates to techniques to generate a sinusoidal signal.

Related Art

[0002] Oscillator devices are well known sources of sinusoidal signals. Some sine-wave oscillators use resonant circuits consisting of inductor and capacitor elements. For example, an LC-tank circuit stores energy alternately in the inductor and capacitor to produce a sine wave. The output frequency of the oscillator is primarily the resonant frequency of the tank circuit and can be represented as:

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Each resonant circuit does, however, contain some resistance which dissipates power. This power loss causes the amplitude to decrease. Loading the tank causes the same effect as increasing the internal resistance of the tank.

[0003] FIG. 1A depicts a prior art oscillator 10. Oscillator 10 may provide a sinusoidal output signal across nodes OUT and OUTN. The peak-to-peak voltage range between the nodes OUT and OUTN of oscillator 10 is limited, in part, to maintain forward voltage biasing of the

diode-like base-collector terminals of the transistors A1 and A2. For example, the maximum peak-to-peak voltage range between the nodes OUT and OUTN of oscillator 10 may be approximately 1.4 volts.

[0004] FIG. 1B depicts another prior art oscillator 20. Oscillator 20 may provide a sinusoidal output signal across nodes OUT and OUTN. The peak-to-peak voltage range between the nodes OUT and OUTN of oscillator 20 is limited, in part, to maintain forward voltage biasing of the diode-like base-collector terminals of the transistors C1 and C2 and the diode-like base-emitter terminals of the transistors B1 and B2. For example, the peak-to-peak voltage range between the nodes OUT and OUTN of oscillator 20 may be approximately 2.8 volts.

[0005] What is needed is a device that provides a sinusoidal signal without the peak-to-peak voltage limitations based on forward biasing diode-like terminals of the transistors utilized in the device.

Brief Description of the Drawings

[0006] The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

[0007] FIGs. 1A and 1B depict prior art oscillators; and

[0008] FIG. 2 depicts a system in which some embodiments of the present invention may be used; and

[0009] FIG. 3 depicts an oscillator in accordance with an embodiment of the present invention.

[0010] Note that use of the same reference numbers in different figures indicates the same or like elements.

Detailed Description

[0011] FIG. 2 depicts one possible system in which some embodiments of the present invention may be used. Receiver 200 may receive signals encoded in compliance for example with optical transport network (OTN), Synchronous Optical Network (SONET), and/or Synchronous Digital Hierarchy (SDH) standards. Example optical networking standards may be described in ITU-T Recommendation G.709 Interfaces for the optical transport network (OTN) (2001); ANSI T1.105, Synchronous Optical Network (SONET) Basic Description Including Multiplex Structures, Rates, and Formats; Bellcore Generic Requirements, GR-253-CORE, Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria (A Module of TSGR, FR-440), Issue 1, December 1994; ITU Recommendation G.872, Architecture of Optical Transport Networks, 1999; ITU Recommendation G.825, "Control of Jitter and Wander within Digital Networks Based on SDH" March, 1993; ITU Recommendation G.957, "Optical Interfaces for Equipment and Systems Relating to SDH", July, 1995; ITU Recommendation G.958, Digital Line Systems based on SDH for use on Optical Fiber Cables,

November, 1994; and/or ITU-T Recommendation G.707, Network Node Interface for the Synchronous Digital Hierarchy (SDH) (1996).

[0012] Referring to FIG. 2, optical-to-electrical converter ("O/E") 255 may convert optical signals received from an optical network from optical format to electrical format. Although reference has been made to optical signals, the receiver 200 may, in addition or alternatively, receive electrical signals from an electrical signal network or wireless or wire-line signals according to any standards. Amplifier 260 may amplify the electrical signals. Clock and data recovery unit ("CDR") 265 may regenerate the electrical signals and corresponding clock and provide the regenerated signals and corresponding clock to layer 2 processor 270. CDR 265 may use some embodiments of the present invention.

[0013] On the regenerated signals, layer two processor 270 may perform media access control (MAC) management in compliance for example with Ethernet, described for example in versions of IEEE 802.3; optical transport network (OTN) de-framing and de-wrapping in compliance for example with ITU-T G.709; forward error correction (FEC) processing, in accordance with ITU-T G.975; and/or other layer 2 processing.

[0014] Interface 275 may provide intercommunication between layer two processor 270 and other devices such as a memory device (not depicted), packet processor (not depicted), microprocessor (not depicted), and/or a switch fabric (not depicted). Interface 275 may provide intercommunication between layer two processor 270 and other devices using an interface that complies with one or more of the following standards: Ten Gigabit Attachment Unit Interface (XAUI) (described in IEEE 802.3, IEEE 802.3ae, and related standards), Serial Peripheral

Interface (SPI), I^2C, CAN, universal serial bus (USB), IEEE 1394, Gigabit Media Independent Interface (GMII) (described in IEEE 802.3, IEEE 802.3ae, and related standards), Peripheral Component Interconnect (PCI), Ethernet (described in IEEE 802.3 and related standards), ten bit interface (TBI), and/or a vendor specific multi-source agreement (MSA) protocol.

[0015] FIG. 3 depicts one implementation of an oscillator 100 in accordance with an embodiment of the present invention. Oscillator 100 may provide a sinusoidal signal having a peak-to-peak voltage range that is not limited by the base-collector diodes of utilized transistors. One implementation of oscillator 100 may include transistors Q1 and Q2, capacitive element C1, inductors L1 and L2, impedance elements 102A and 102B, and current source 106. Output terminals OUT and OUTN of oscillator 100 may provide a sinusoidal signal. Of course other implementations may be used.

[0016] Transistors Q1 and Q2 may be implemented as bipolar junction transistor (BJT) devices having similar characteristics. Other types of transistors may be used. Inductors L1 and L2 may couple a bias voltage Vh to collector terminals of respective transistors Q1 and Q2. In one implementation, inductors L1 and L2 may have approximately the same inductance values. Emitter terminals of transistors Q1 and Q2 may be coupled to current source 106. Impedance element 102A may couple a base terminal of transistor Q1 to terminal OUT. Impedance element 102B may couple a base terminal of transistor Q2 to terminal OUTN. In one implementation, impedance elements 102A and 102B may have approximately the same impedance values. In one implementation, each of impedance elements 102A and 102B may be implemented as a capacitive element in parallel with a resistive element. Impedance elements 102A and 102B do not load the LC tank, thereby providing an improvement over the well-known Clapp

configuration. In the Clapp configuration, a resistive biasing is in parallel with the LC tank, thus adding load to the LC tank. Utilizing high resistance and capacitances in the impedance elements 102A and 102B may increase the range of peak-to-peak voltages that can be provided by nodes OUT and OUTN. Capacitive element C1 may couple node OUTN to node OUT.

[0017] The frequency of a sinusoidal signal provided by nodes OUTN and OUT may be defined by:

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

where L is the impedance of L1 and

C is the capacitance of capacitive element C1.

[0018] The impedance elements 102A and 102B may control a peak-to-peak range of sinusoidal voltages provided between nodes OUT and OUTN. When a peak voltage is provided at node OUT, there is a voltage build-up across impedance element 102A prior to settling the base terminal voltage of transistor Q1. The voltage build-up across impedance element 102A extends a voltage peak that can be applied at node OUTN and maintain an operating base terminal voltage of transistor Q1. Settling a bias voltage at the base terminal of transistor Q1 may cause the voltage at node OUTN to go to a peak value, which leads to a voltage build-up across impedance element 102B. A voltage build-up across impedance element 102B extends a voltage peak that can be applied at node OUTN and maintain an operating base terminal voltage of transistor Q2. The impedance elements 102A and 102B thereby provide for an extended peak-to-peak voltage oscillation range at least over those of oscillators 10 and 20.

[0019] For example, in one implementation, terminals OUT and OUTN may provide a sinusoidal voltage signal having a peak-to-peak swing of approximately 3.75 volts. In this implementation, impedance elements 102A and 102B each have a resistance component of approximately 10 kiloohms in parallel with a capacitance of 10 nanofarads (nF); the inductance of each of inductors L1 and L2 may be approximately 10 micro Henry (mH); a bias voltage of approximately 3.3 volts; a capacitance of capacitive element C1 may be 1 nanofarads (nF); and the current source 106 may provide a current of 2 milliamperes (mA). Of course, other parameters may be used.

Modifications

[0020] The drawings and the forgoing description gave examples of the present invention. The scope of the present invention, however, is by no means limited by these specific examples. Numerous variations, whether explicitly given in the specification or not, such as differences in structure, dimension, and use of material, are possible. The scope of the invention is at least as broad as given by the following claims.